What is Claimed is:

[c1] An apparatus for reading out multiple match hits from a content addressable memory (CAM), comprising:

a priority encoder for receiving a plurality of matchlines from a CAM and for encoding addresses of the CAM that are associated with the matchlines that indicate a match; and

a matchline mask system for selectively masking off a matchline that indicates a match from the priority encoder after the address associated with that matchline is encoded by the priority encoder.

[c2] The apparatus according to claim 1, wherein the matchline mask system comprises:

a plurality of matchline mask units, wherein each matchline passes through a corresponding one of the matchline mask units.

[c3] The apparatus according to claim 2, further comprising:

a decoder system for selecting the matchline mask unit corresponding to the encoded address output by the priority encoder.

[c4] The apparatus according to claim 3, wherein the decoder system comprises:

a plurality of decoders, wherein each decoder is associated with one of the matchline mask units.

[c5] The apparatus according to claim 3, wherein each matchline mask unit comprises:

a flip-flop having an output and a set input for receiving a mask off signal from the decoder system, wherein, in response to the mask off signal, the output of the flip-flop sets the matchline associated with the matchline mask unit to a no-match condition.

[c6] The apparatus according to claim 5, wherein the mask off signal is provided to the set input of the flip-flop through a FET, and wherein a gate of the FET is controlled by a clock signal.

[c7] The apparatus according to claim 5, wherein the matchline passes through a FET, and wherein the output of the flip-flop controls the gate of the FET to

disconnect the matchline entering the matchline mask unit from the matchline exiting the matchline mask unit in response to the mask off signal.

[c8] The apparatus according to claim 5, wherein the output of the flip flop controls the gate of a FET that is connected to the matchline and a voltage level indicative of a no-match condition, and wherein the matchline is set to the voltage level in response to the mask off signal.

[c9] The apparatus according to claim 1, further comprising:

a match counter for providing a current match count and a no match flag.

[c10] The apparatus according to claim 1, wherein the priority encoder sequentially encodes the address associated with each matchline that indicates a match, and the matchline mask system sequentially masks off the associated matchline, until none of the matchlines indicates a match.

[c11] An apparatus for masking matchlines of a content addressable memory (CAM), comprising:

a plurality of matchline mask units, wherein each matchline of the CAM passes through a respective one of the matchline mask units, and wherein each matchline mask unit is configured to mask its associated matchline from a priority encoder; and

a decoder system for sequentially masking each matchline that indicates a match from the priority encoder using the matchline's respective matchline mask unit.

[c12] The apparatus according to claim 11, wherein the priority encoder encodes a CAM address for each matchline that indicates a match, and wherein the decoder system selects a matchline to be masked in response to the priority encoder encoding a CAM address that is associated with the matchline.

[c13] The apparatus according to claim 11, wherein each matchline mask unit comprises:

a flip-flop having an output and a set input for receiving a mask off signal from the decoder system, wherein, in response to the mask off signal, the output of the flip-flop sets the matchline associated with the matchline

mask unit to a no-match condition.

[c14] The apparatus according to claim 13, wherein the mask off signal is provided to the set input of the flip-flop through a FET, and wherein a gate of the FET is controlled by a clock signal.

[c15] The apparatus according to claim 13, wherein the matchline passes through a FET, and wherein the output of the flip-flop controls the gate of the FET to disconnect the matchline entering the matchline mask unit from the matchline exiting the matchline mask unit in response to the mask off signal.

[c16] The apparatus according to claim 13, wherein the output of the flip flop controls the gate of a FET that is connected to the matchline and a voltage level indicative of a no-match condition, and wherein the matchline is set to the voltage level in response to the mask off signal.

[c17] A method for reading out multiple match hits from a content addressable memory (CAM), comprising:

receiving a plurality of matchlines from a CAM;

determining and prioritizing the matchlines that indicate a match;

sequentially encoding the addresses of the CAM that are associated with the matchlines that indicate a match; and

selectively masking off a matchline that indicates a match after the address associated with that matchline has been encoded.

[c18] The method of claim 17, wherein the plurality of matchlines initially indicate a total of M matches, and wherein the total number of matches is reduced by 1 each time an address is encoded.

[c19] The method of claim 17, wherein the masking reduces a minimum cycle time between the encoding of addresses in the CAM.